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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,110	07/21/2000	Charles Cohn	6-4	4412

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EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/621,110	Applicant(s) COHN ET AL.	
	Examiner Chuong A Luu	Art Unit 2814	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

The Rejections

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Banerjee et al. (U.S. 6,440,770 B1)

Banerjee discloses an integrated circuit package with

(1) (a) forming a substrate having a first dielectric layer, a conductive layer having a first region insulated from a second region and located above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric

layer having a cavity wherein the first and second regions are exposed within the cavity and the first region insulated from the second region by a third dielectric layer;

(b) interconnecting a first lead of an integrated circuit to the first exposed region and interconnecting a second lead of the integrated circuit to the exposed second region (see column 2, lines 40-48; column 3, lines 36-57. Figure 1);

(2) wherein step (b) comprises: coupling a conductor to a bond pad formed on the integrated circuit; connecting the conductor directly to the conductive layer (see column 3, lines 36-44);

(3) further comprising providing one of a ground plane and a power plane in the exposed portion of the conductive layer (see column 3, lines 64-66);

(4) further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer (see column 3, lines 64-66);

(5) further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer (see column 3, lines 64-66);

(6) further comprising forming multiple interconnections between the integrated circuit chip and the conductive layer (see Figure 1).

(7) (a) forming a first dielectric layer on a substrate;

(b) forming a conductive layer having a first region insulated from a second region above the first dielectric layer;

(c) a second dielectric layer above the conductive layer;

(d) forming a cavity in the second dielectric layer to expose the first and second regions of the conductive layer and coupling a first lead of the integrated circuit chip to

the exposed first region and coupling a second lead of the integrated circuit to the exposed second region, the first region insulated from the second region by a third dielectric layer (see column 2, lines 40-48; column 3, lines 36-57. Figure 1);

(8) wherein steps (a), (b), and (c) occur prior to step (d) (see Figure 1);

(9) further comprising: providing a contact area to a ground plane by exposing the portion of the conductive layer (see column 3, lines 64-66);

(10) (e) forming plated through holes in the substrate (see Figure 1);

(12) further comprising coupling the integrated circuit chip to the substrate (see Figure 1);

Allowable Subject Matter

Claims 13-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or suggest inter alia the limitations "forming a second conductive layer above the second dielectric layer and forming a cavity in the first region of the second dielectric layer to expose the first and second regions of the first conductive layer and coupling a first lead of the integrated circuit to the exposed first region and a second lead of the integrated circuit to the exposed second region".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

C. Everhart
CARIDAD EVERHART
PRIMARY EXAMINER

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March 7, 2003